

IN THE CLAIMS:

Claim 1. (Currently Amended) A method for prefetching instructions and data of a program stored in a main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the at least one instruction or an address for data, the method comprising the steps of:

reading the program from the main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction and an address for data;

detecting the pseudo instruction with a first unit;

reading the instruction ~~or~~ and the data from the main memory in accordance with the address for the instruction ~~or~~ and the address for the data with the first unit when the pseudo instruction is detected;

storing the instruction ~~or~~ and the data in a buffer; and

executing the stored instruction with a second unit.

Claim 2. (Currently Amended) The method of claim 1, wherein the first unit includes a pseudo instruction detection unit connected in parallel with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the main memory to the pseudo instruction detection unit in parallel with the buffer.

Claim 3. (Currently Amended) The method of claim 1, wherein the buffer includes first and second buffers connected in parallel to the main memory, and the method further comprising a step of storing the instruction and data read from the main memory in the first buffer and storing the instruction ~~or~~ and the data included in the detected pseudo instruction in the second buffer.

Claim 4. (Currently Amended) The method of claim 3, further comprising the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction ~~or~~ and the data from the main memory in accordance with the at least one instruction address ~~or~~ and the data address with the first unit after the transfer of the at least one instruction to the first buffer has been identified.

Claim 5. (Currently Amended) The method of claim 4, further comprising the step of identifying that the corresponding instruction ~~or~~ and data is are stored in the second buffer in accordance with the at least one instruction address ~~or~~ and the data address when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction ~~or~~ and data is are not stored in the second buffer.

Claim 6. (Currently Amended) The method of claim 1, further comprising the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction ~~or~~ and the data from the main memory in accordance with at least one instruction address ~~or~~ and data address with the first unit after the transfer of at least one instruction to the buffer has been identified.

Claim 7. (Currently Amended) The method of claim 6, further comprising the step of identifying that the corresponding instruction ~~or~~ and data is are stored in the buffer in accordance with the at least one instruction address ~~or~~ and data address with the first unit when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction ~~or~~ and data is are not stored in the buffer.

Claim 8. (Currently Amended) A microcontroller, comprising:
a buffer, connected to a main memory, for storing ~~instructions and data of~~ a program read from the main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the ~~at least one instruction~~ ~~or~~ and an address for data;

a first unit including,

✓ a pseudo instruction detection unit, connected to the main memory, for detecting the pseudo instruction included in the program read from the main memory; and

an address control unit, connected to the ~~external~~ main memory and the pseudo instruction detection unit, for reading the instruction ~~or~~ and data from the main memory in accordance with the address for the instruction ~~or~~ and the address for the data when the pseudo instruction is detected and storing the instruction ~~or~~ and the data in the buffer; and

a second unit connected to the buffer, for executing the instruction stored in the buffer.

④ Claim 9. (Currently Amended) The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel to the main memory, wherein the first buffer stores the instruction and data read from the main memory, and the second buffer stores the instruction ~~or~~ and data included in the detected pseudo instruction.

Claim 10. (Currently Amended) The microcontroller of claim 9, wherein the address control unit identifies that the corresponding instruction ~~or~~ and data ~~is~~ are stored in the second buffer in accordance with the at least one instruction address ~~or~~ and data address when the pseudo instruction is detected and permits storage of the instruction ~~or~~ and the data in the second buffer when the corresponding instruction ~~or~~ and data ~~is~~ are not stored in the second buffer.

Claim 11. (Currently Amended) The microcontroller of claim 10, wherein the pseudo instruction detection unit is connected in parallel with the first buffer for the main memory.

Claim 12. (Currently Amended) The microcontroller of claim 8, wherein the address control unit identifies that the corresponding instruction ~~or~~ and data ~~is~~ are stored in the buffer in accordance with the at least one instruction address ~~or~~ and data address when the pseudo instruction is detected and permits storage of the instruction ~~or~~ and the data in the buffer when the corresponding instruction ~~or~~ and data ~~is~~ are not stored in the buffer.

Claim 13. (Currently Amended) The microcontroller of claim 12, wherein the pseudo instruction detection unit is connected in parallel with the buffer for the main memory.

Claim 14. (Currently Amended) A device for detecting a pseudo instruction present before a specific instruction, wherein the pseudo instruction is stored in a main memory and includes an opcode and an operand, and wherein the device is independent of an instruction execution unit for executing the specific instruction, the device comprising:

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a detection circuit, connected to ~~a data line~~ the main memory, for receiving the pseudo instruction ~~transferred on the data line~~ read from the main memory and detecting the opcode included in the pseudo instruction; and

✓
a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode when the pseudo instruction is detected and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

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Claim 15. (Cancelled)

Claim 16. (Currently Amended). A microcontroller connected to a main memory which stores a program including instructions and data, the microcontroller comprising:

an instruction execution unit for reading instructions and data from the main memory and processing the read instructions; and

a prefetch circuit unit that receives instructions and data read from the main memory in response to a fetch signal, and detects pseudo instructions included in the instructions and data, wherein a pseudo instruction precedes a branch instruction and indicates the existence of the branch instruction, and wherein the prefetch circuit is independent of the instruction execution unit;

wherein the prefetch circuit unit includes,

a prefetch buffer connected between the instruction execution unit and the main memory for temporarily storing instructions and data being transferred from the main memory to the instruction execution unit,

a bus interconnecting the prefetch buffer and the main memory,

a pseudo instruction detection unit connected to the bus for detecting pseudo instructions among the instructions and data being transferred from the main memory to the prefetch buffer,

a holding circuit, connected to the bus and to the pseudo instruction detection unit, for storing operands of the pseudo instruction,

a pseudo instruction buffer for temporarily storing instructions and data fetched from a location in the main memory which is pointed to by the branch instruction following the pseudo instruction,

an address control unit for generating the fetch signal and for generating a main memory address which points to the address of a next word to be read from the main memory, and wherein when the pseudo instruction detection unit detects a pseudo instruction, the instructions and data pointed to by the pseudo instruction are fetched from the main memory by the address control unit and stored in the pseudo instruction buffer so that when the branch instruction following the pseudo instruction is processed by the instruction execution unit, if the branch is taken, the instructions and data pointed to by the branch instruction have been prefetched and stored in the pseudo instruction buffer.

Claim 17. (Currently Amended) The microcontroller of claim 16, wherein the pseudo instruction detection unit further comprises:

a pseudo instruction detection circuit that receives at least a part of each of the instructions and data being transferred from the main memory to the prefetch buffer, detects an opcode of a pseudo instruction therefrom, and generates a detection signal; and

a shift register connected to the pseudo instruction detection circuit and receiving the detection signal, and generating a hold circuit enable signal, wherein when the hold circuit enable signal is active, the holding circuit stores the pseudo instruction operands being transferred on the bus.

Claim 18. (Currently Amended) The microcontroller of claim 17, wherein the holding circuit includes:

an additional information holding circuit that stores a first operand of the pseudo instruction;

an upper address holding circuit that stores a second operand of the pseudo instruction; and

a lower address holding circuit that stores a third operand of the pseudo instruction, wherein the second and third operands comprise a main memory address.

Claim 19. (Cancelled)

Claim 20. (Cancelled)

Claim 21. (Cancelled)

Claim 22. (Cancelled)

Claim 23. (Cancelled)

Claim 24. (Previously Presented) The method of claim 1, wherein the at least one instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

Claim 25. (Currently Amended) The method of claim 1, further comprising ~~executing~~ handling the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected.

Claim 26. (Currently Amended) The method of claim 1, further comprising the second unit ignoring an address for the pseudo instruction when receiving the address for the at least one instruction ~~or~~ and the address for data to skip the pseudo instruction.

Claim 27. (Previously Presented) The microcontroller of claim 8, wherein the at least one instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

Claim 28. (Currently Amended) The microcontroller of claim 8, wherein the second unit ~~executes~~ handles the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected.

Claim 29. (Currently Amended) The microcontroller of claim 8, wherein the second unit ignores an address for the pseudo instruction when receiving the address for the at least one instruction ~~or~~ and the address for data to skip the pseudo instruction.

Claim 30. (Currently Amended) A method for prefetching ~~instructions and data~~ of a program stored in a main memory, ~~wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data,~~ the method comprising the steps of:

reading the program from the main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction and an address for data;

detecting the pseudo instruction with a first unit;

prefetching the instruction ~~or~~ and data in accordance with the detection of the pseudo instruction with the first unit when the pseudo instruction is detected; and

~~executing~~ handling the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected with a second unit.

Claim 31. (Currently Amended) A method for prefetching instructions and data of a program stored in a main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the method comprising the steps of:

reading the program from the main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction and an address for data;

detecting the pseudo instruction with a first unit when the pseudo instruction is detected;

prefetching the instruction or and data in accordance with the detection of the pseudo instruction with the first unit; and

when receiving the address for the at least one instruction or and the address for data a second unit, which is independent of the first unit, skipping the pseudo instruction and executing the prefetched instruction.

Claim 32. (Currently Amended) An apparatus for prefetching instructions and data of a program stored in a main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

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a first unit for reading the program from the main memory ~~and detecting the pseudo instruction, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, and wherein the first unit detects the pseudo instruction and prefetches the instruction or and data when the pseudo instruction is detected;~~ and

a second unit for executing a no-operation (NOP) operation in accordance with the detection of the pseudo instruction.

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Claim 33. (Currently Amended) An apparatus for prefetching ~~instructions and data of a program stored in a main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data,~~ the apparatus comprising:

a first unit for reading the program from the main memory ~~and detecting the pseudo instruction, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, and wherein the first unit detects the pseudo instruction and prefetches the instruction or and data when the pseudo instruction is detected;~~ and

a second unit for executing the prefetched instruction, wherein the second unit ignores an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data to skip the pseudo instruction.

Claim 34. (Currently Amended) ~~An apparatus for prefetching instructions and data of a program stored in a main memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:~~

~~a first unit for reading the program from the main memory and detecting the pseudo instruction, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, and wherein the first unit reads the instruction or and data from the main memory in accordance with the address for the instruction or and the address for the data when the pseudo instruction is detected, wherein the first unit includes a buffer for storing the instruction or and the data;~~
and

a second unit for executing the stored instruction.